A 2GHz Compact 60W Fully Integrated 3-Way Doherty for Simultaneous Dual-Band Operation

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***Abstract* — This paper presents the design approach, realization and measurement results of a compact driver multi-stages 3-way fully integrated Doherty MMIC 60W power amplifier for true dual-band operation using LDMOS technology. Those results are achieved thanks to the C_{ds} cancellation technic for the combiner design to achieve wideband impedance transformation combined with the 3-way DPA architecture to reach high efficiency in deep back-off and reduce load modulation. Through this design a dedicated attention is put to extend PA video bandwidth thanks to integrated passive device to handle simultaneous digital pre-distortion linearization in B1 and B3, 4G/4.5G telecommunication band. This device is highly linear, after digital pre-distortion ACLR of -56dBc are measured for 2cLTE 20MHz 8dB PAR spaced by 345MHz at 35dBm, 12dB OBO, while efficiency is above 29%. Moreover, LDMOS technology is a mature process, consequently this MMIC is a reliable low-cost PA solution for mass production in a very compact package.**

***Keywords* — 3-way Doherty, LDMOS, power amplifiers, 4.5G, MMIC, DPD.**

I. INTRODUCTION

Despite the roll out of the fifth generation (5G) active antenna unit (AAU), the existing 4G/4.5G network need to be maintained and still represent a big market in telecommunication industry. Base station (BTS) equipment manufacturers require higher efficiency with ultra-wide instantaneous bandwidth while costs reduced compared to the previous PA generation. One solution to lower BTS cost at 2GHz is to have PA capable to handle simultaneously B1 and B3 telecommunication band with high linearity. Using a device that allows concurrent dual band capability reduces the total transceiver line up by two which means multiple benefits for manufacturers. Additionally to cost reduction, it's interesting for the total BTS power consumption and allows a better compactness. Achieving high efficiency over a wide instantaneous bandwidth remains the most difficult challenge for realizing power amplifiers, mostly in Silicon LDMOS technology, due to drain to source capacitance. Conventional Doherty power amplifiers (DPA), which utilize the concept of active load modulation, have been used since decades in base station due to their advantages to deal with high peak to average ratio (PAR) modulated signal [1]-[2]. However nowadays, 2-way symmetric DPA suffer from efficiency and 2-way asymmetric DPA have several limitations in linearity and bandwidth to address true dual band application using LDMOS. After a study between different N-way DPA architecture, a 3-way architecture with the adapted ratio between carrier, peak 1 and peak 2 transistors demonstrates the capability to achieve higher efficiency compared to an asymmetric DPA while assuming good linearity with a limited load modulation for wideband capability. Moreover, to achieve a wider PA impedance transformation, the C_{ds} cancellation technic [3] is used to realize the combiner of the device. Other benefit of this method is the DPA is fully integrated in a single compact package which reduces the size of the device.

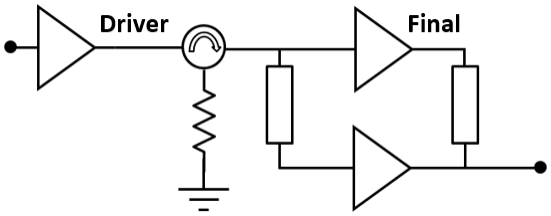

Fig. 1. Transceiver PAs Line-up

Nowadays miniaturization and integration are key for BTS. In fact, like display on Fig. 1 it's easy to understand that lot of footprint on PCB is gained using a single package instead of dual path or to make the DPA matching on PCB. In this paper a fully integrated low-cost driver solution using LDMOS technology is proposed to enhance efficiency with high linearity for dual band B1 and B3 application. The device is a 60W 3-way fully integrated DPA at 2GHz capable to achieve more than 29% efficiency during a simultaneous transmission of a pairs of 20 MHz LTE signals spaced by 345MHz meaning an instantaneous bandwidth (IBW) for the PA of 385 MHz. After digital pre-distortion ACPR are lower than -56dBc at 35dBm, 12dB OBO. Thanks to a big focus during design optimization the PA has an extended video bandwidth above to 600MHz at 38 dBm for high linearity which is really challenging for this kind of power and multi-stage architecture.

II. COMPACT INTEGRATION OF 3-WAY DOHERTY

A. 3-Way Doherty Concept

For cost reasons, BTS equipment manufacturers require PAs capable to handle wide telecommunication bands on a large spectrum, mostly 400MHz while maintaining high linearity and efficiency. To combine those performances, a 3-

way Doherty is proposed. In fact, from theoretical and measured studies [3] comparing the traditional DPA currently designed in the semiconductor industry, 3-way DPA can achieve better efficiency with reduced load modulation to overcome bandwidth limitations. Moreover, it has been proofed that the 3-way integrated DPA architecture [5] is suitable for multiband application at those frequencies. The 3-way implemented DPA concept in Fig. 2 implies new challenges to face.

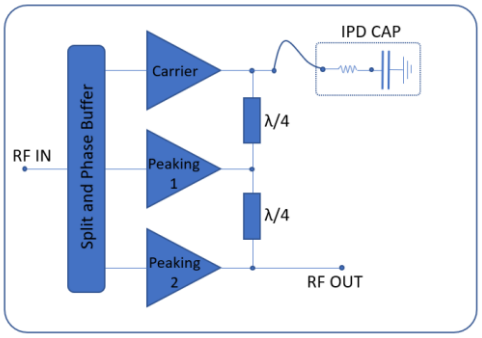

Fig. 2. 3-way integrated DPA configuration with IPD

The realization of the output combiner is the keystone of DPA. In fact, impedances presented by the integrated matching to each different transistor have to be perfectly optimized over the bandwidth. The combiner is made thanks to the C_{ds} cancellation technic which will be described in the next section.

The input splitter follows the combiner design. It's fully integrated on the same silicon die. Main challenges during design are the phase delay and power splitting that have to be optimized for optimum DPA operation.

B. *Cds cancellation technic*

A common method employed to manage parasitic transistor LDMOS C_{ds} is the cancelation using a shunt inductor. However, it involves the presence of additional wires (used as inductors), that generate mutual coupling with input/output wires and add parasitic losses. The C_{ds} cancellation technic [3]-[4]-[5] is based on using the C_{ds} parasitic value of each transistor, main and peak, into the combiner design to realize the equivalent transmission line structure to work as an impedance inverter (Fig. 3).

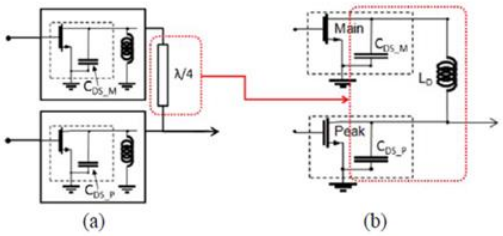

Fig. 3. (a) Impedance inverter using a quarter wave transmission line and (b) Integrated compact combiner Cds_M-Ld-Cds_P Pi filter

This is a Pi filter topology where L_d inductance is realized with high Q wires to limit efficiency losses. At 2GHz, wavelength and 3-way DPA architecture are a real challenge to handle due to long wires that generates some interaction with input wires (wire height, coupling effect).

III. Extended Video Bandwidth

A. *Integrated Passive Device*

One of the main well-known challenge for RF industrial PAs is to be linearized for wideband telecommunication signal with high efficiency. However, linearity and efficiency are opposite performances. First main challenge for designer is to optimize RF performances in band. First criterion is to have a DPA with a flat large small signal gain (over 400MHz). Then to have a reduce gain, power and phase dispersion over frequencies. Those conditions will allow to limit short term memory effect which are short time constant. This memory effects are mostly corrected by current digital pre-distortion algorithm. Unfortunately, long term memory effects associated to the bias networks are one of the main limitations for linearization because they are very difficult to predict and model. Especially when the resonance frequency of these networks is in the same range as the baseband envelope frequency of the input signal. That's why during the design flow baseband resonances and impedances must be optimized. Moreover, the intrinsic parasitic resonances increase with transistor size, so in other words with power. To optimize baseband impedance and push the low frequency resonance (LFR) at higher frequency, an integrated passive device (IPD) is integrated inside the package. The IPD circuit is based on a separated silicon die interconnected to the Doherty MMIC trough bond-wires (Fig. 2). The circuit implements a high value capacitor (some nF) and a series resistor. The resistor plays as a dumping network to remove the parasitic self-resonance of the bond-wires and the capacitor. The presence of this energy tank close to the Carrier of the Doherty increase considerably the low frequency resonance of the whole Doherty boosting the IBW higher than 350 (MHz).

At 2GHz frequency due to wavelength, it's really challenging to integrate this into the package without creating coupling effect with 3-way integrated DPA combiner wires.

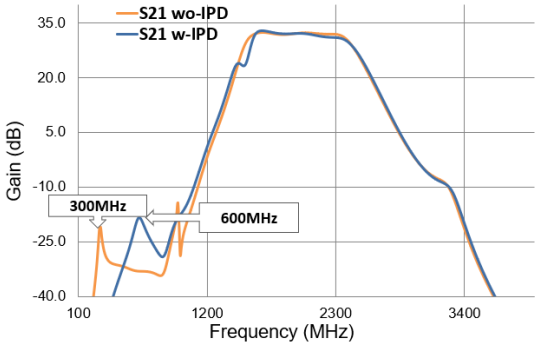

Fig. 4. Simulated S-Parameters with and without IPD

As display into the Fig. 4 the integration of IPD allows to have a higher LFR and lower baseband impedance which extends video-bandwidth and it makes favourable for wideband linearization.

IV. Measurement Results

A. RF Performances

The PA is assembled in a low-cost reliable compact solution, OMP400 package. The overall circuit is implemented on a printed circuit board (PCB) using an RO4350B substrate of 20mils thickness. Copper baseplate for heat dissipation is soldered directly at the backside of the PCB as shown in Fig. 5. The effective matching area is compact, 18 x 22cm and only two gate biases are used to supply carrier, peak 1 and peak 2 amplifiers to be more compact and easier to integrate. Measurements are performed at ambient temperature 25°C. V_{ds} voltage is set to 28V while Vgs_c is set at 2.19V to regulate the quiescent current at 100mA.

For measurement, the MMIC is tuned on maximum power impedance location for linearization capability in 1805-2170MHz band to handle B1 and B3 simultaneously.

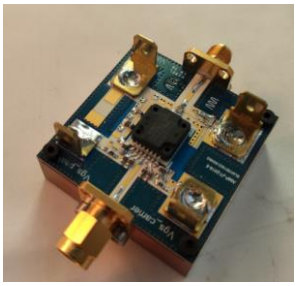

Fig. 5. Printed Circuit Board, effective area 18 x 22 cm

S-parameters measurement in Fig. 6 confirms that 3-way DPA can achieve wide bandwidth and has a flat gain over 400MHz and the LFR is pushed close to 600MHz which eases the DPD linearization.

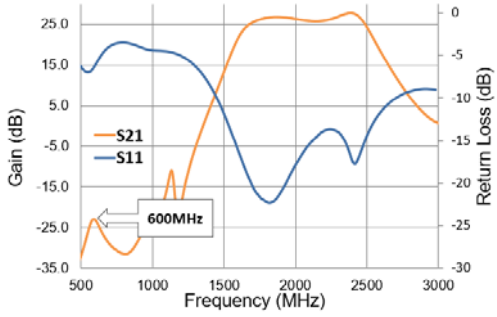

Fig. 6. Measured S-Parameters on the board

This result is only possible by the adding of IPD inside the MMIC, without it the LFR drops lower and the baseband impedance is higher which is one the main limitation for DPD correction. The input is well matched, as shown by a return loss closed to -15dB from 1.8GHz to 2.17GHz.

AM-AM results (Fig. 7) confirms the capability of a 3-way integrated DPA to be wideband over 400MHz bandwidth and linear thanks to the reduce load modulation. Indeed, there is a minimum gain spread less than 1 dB at the operating power with a high gain of 27 dB. Efficiency is above 27% at 12dB OBO over frequencies. Moreover, compression is smooth, P1dB is closed to P3dB over the full band. This result confirms that this PA is suitable for driver application.

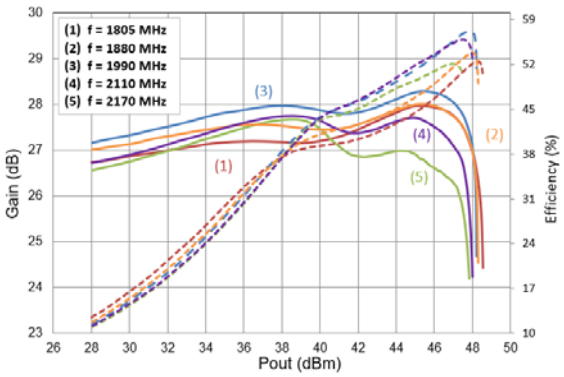

Fig. 7. AM-AM and Efficiency

The video bandwidth is measured at 38dBm (3dBm margin higher than the real operating power), IMD3 resonance. This measurement is performed thanks to two-tones CW with various spacing with a constant output power.

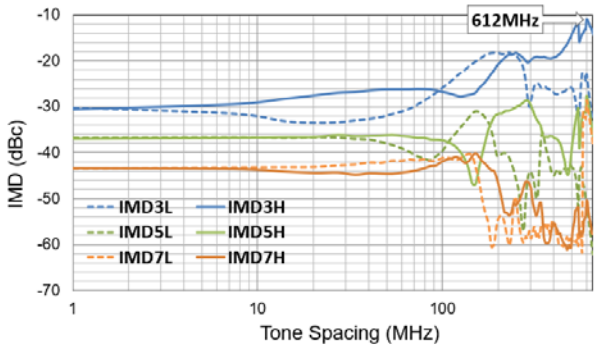

Fig. 8. IMDs at 38dBm output power for various two-tones spacing with center frequency 1990MHz

The figure of merit, Fig. 8, shows a resonance above 600MHz. It's well known that this resonance is linked with envelope impedance in baseband (LFR). Thanks to IPD optimization the VBW is extended twice compared without this resonating network. This result is outstanding for this kind of power, 60W in fully integrated package with this complex architecture, 3-way DPA.

This result combined with the LFR pushed at higher frequency is favorable for managing dual-band linearization modulated signal with very high spacing, up to 345MHz, as required by the application.

B. Digital Pre-Distortion correction results

Linearization is performed with different spacing for 2cLTE 20MHz with 8dB PAR at 12dB OBO, 35dBm. This is the typical test case scenario requested by BTS equipment manufacturers for 2GHz true dual band application. Moreover, to also proof the PA capability for multiband application, 3cLTE 20MHz 8dB PAR modulated signal at the operating power is linearized on B1, B2 and B3 band.

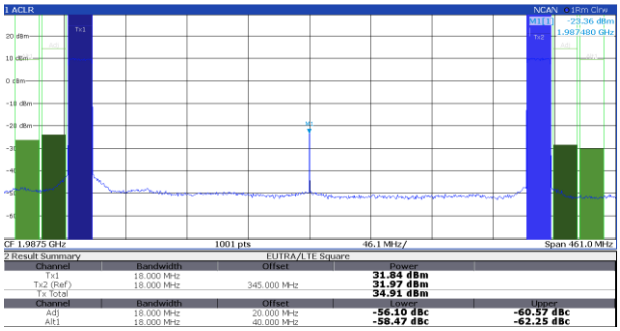

Fig. 9. ACLR result after DPD correction

Result in Fig. 9 displays ACLR below -56dBc after DPD correction with an efficiency measured at 29%. This performance demonstrates that this PA is highly linear and can handle B1 and B3 band simultaneously. Moreover, with dedicated DPD (dual engine DPD) -60dBc can be reach at 38dBm for the same signal.

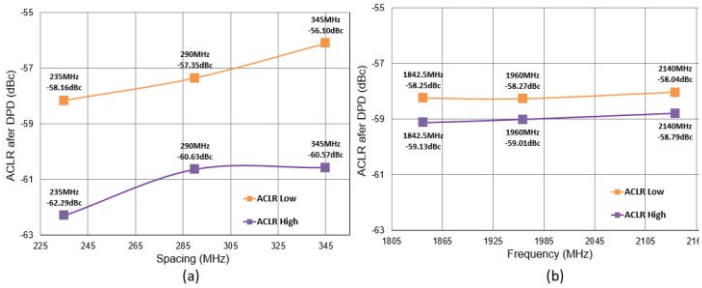

Fig. 10. ACLR result after DPD correction (a) 2cLTE 20MHz vs Spacing and (b) 3cLTE 20MHz vs B1, B2 and B3 band

As expected, this PA is also suitable for multiband driver application, it's highly linear, always above -58dBc (Fig. 10.b) for 60MHz IBW in each sub-band B1, B2 and B3.

Table 1. Performance comparison Doherty PA design for 2GHz

Freq	1.8-2.2GHz	1.805-1.88GHz	1.8-2.2GHz	1.8-2.2GHz
Pavg	39dBm	44.5dBm	47.3dBm	35dBm
Max Gain	16.7dB	20.3dB	15dB	27dB
ACLR DPD for 3cLTE*	-57.01/-54.58dBc (B2)	-51.22/-52.08dBc (B3)	NA	-58.04/-58.79dBc (B1)
ACLR DPD for 2cLTE spaced*	Single band	Single band	-54.1/-52.3dBc (B1+B66)	-56.10/-60.57dBc (B1+B3)
DPD Eff	47% (8dB OBO)	50% (8dB OBO)	44.3% (8dB OBO)	29% (12dB OBO)
Doherty Type	3-way iDPA	2-way DPA	2-way DPA	3-way iDPA
Techno	LDMOS	LDMOS	GaN	LDMOS
Reference	[5]	[6]	[7]	T.W

*DPD results displayed are for the worst case in each case (B1, B2, B3 or spacing).

From literature (Table 1) many focuses was put on final stage PAs to address multiband/dual band application at 2GHz in LDMOS and GaN. It appears that GaN solution is the easiest technology solution to address this concurrent dual band final application for high power due to low C_{ds}. This PA represents the best compromise among linearity, efficiency and compactness. In fact, the total line-up linearized efficiency at 8dB OBO of this DPA and final GaN [7] is 41%. Whereas for traditional Class AB driver PA [8] total efficiency is only 38% for a larger matching area. This work is, from the best author's knowledge, the first 3-way multi-stage fully integrated DPA to address simultaneously two sub-band application at 2GHz in LDMOS.

V. Conclusion

A low cost compact reliable 60W fully integrated 3-Way Doherty PA for true dual band application at 2GHz is presented. The integrated combiner is realized thanks to C_{ds}-L_d-C_{ds} Pi filter to achieve wideband impedance transformation. To extend video bandwidth integrated passive device are put inside the MMIC with a big optimization focus to avoid coupling effect. It shows that IPD can push the LFR by twice. Measurements demonstrates the capability of this recent architecture to achieve high linearity with good efficiency in deep back of for simultaneous DPD in B1 and B3 band with LTE modulated signal with a fully integrated solution. This architecture used for driver PA allows to increase efficiency and reduced cost of the overall line-up. In comparison with other DPA solutions at 2GHz, this state of the art 3-way LDMOS integrated DPA presented is one of the only RF industry solution to manage true dual band operation.

References

[1] A. Grebennikov and S. Bulja, "High-Effciency Doherty Power Amplifers: Historical Aspect and Modern Trends," *Proc. Of the IEEE*, vol. I00, no.12, pp.3190-3219, Dec. 2012.

[2] John R. Gajadharsing, "Recent advances in Doherty amplifiers for wireless infrastructure", *IEEE MTT-S Int. Microw. Symp. Workshop*, June 2009.

[3] "A Compact 60 W MMIC Amplifier based on a Novel 3-Way 1:2:1 Doherty Architecture with Best-in-Class Efficiency for Small Cells", *IEEE MTT-S IMS Symposium*, June 2017.

[4] Xavier Moronval, John R. Gajadharsing, "A 100 W Multi-Band Four-Way Integrated Doherty Amplifier", *IEEE MTT-S IMS Symposium*, May 2016.

[5] H. Zhang, S. De Meyer, C. Duvanaud, S. Bachir, "A 50W highly linear 3-way Integrated Wideband Doherty PA for Small-Cell Application", *13th EuMIC*, 2018.

[6] A. Xu, M. Lu, E. Wang, "A 150W High Efficiency Integrated Doherty Amplifier for LTE-Advanced Applications", *IEEE MTT-S IMS Symposium*, June 2018.

[7] N. Zhu, R. McLaren, J S. Roberts, D. Holmes, M. Masood, J K. Jones, "Compact High Efficiency High-Power Wideband GaN Amplifier Supporting 395 MHz Instantaneous Bandwidth", *IEEE MTT-S IMS Symposium*, June 2019.

[8] "BLM7G1822S-40PB data sheet", Ampleon, Netherland.