Three dimensional nanoscale mapping of state of the art finFETs

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**S1. Atom probe tomography for NMOS: maps for other species**

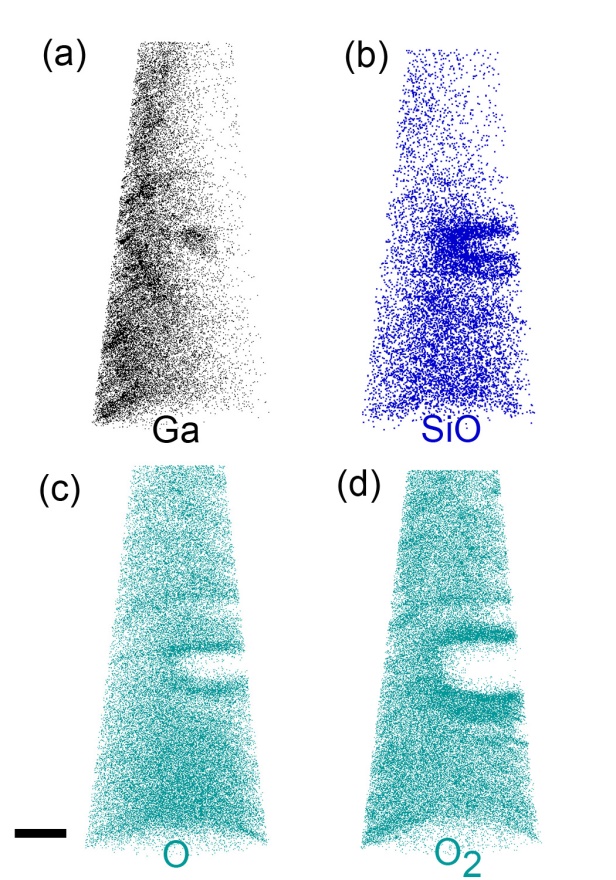


Figure S1: APT maps of Ga, SiO, O, and O2 for a NMOS fin. (a) The Ga is from contamination during the ion milling process in the FIB (focused ion beam). The milling conditions used is to ensure that minimum Ga damage occurs during the sample tip preparation. (b) The SiO maps show a higher concentration close to the fin (Figure 3 (a) main text) due to close proximity of Si and O (from the HfO2 layer). (c, d) The O and O2 maps are also shown. The O maps show a higher concentration close to the interface of the fin and the HfO2 dielectric. Scale bar is 25 nm.

**S2. Atom probe tomography for PMOS: maps for other species**

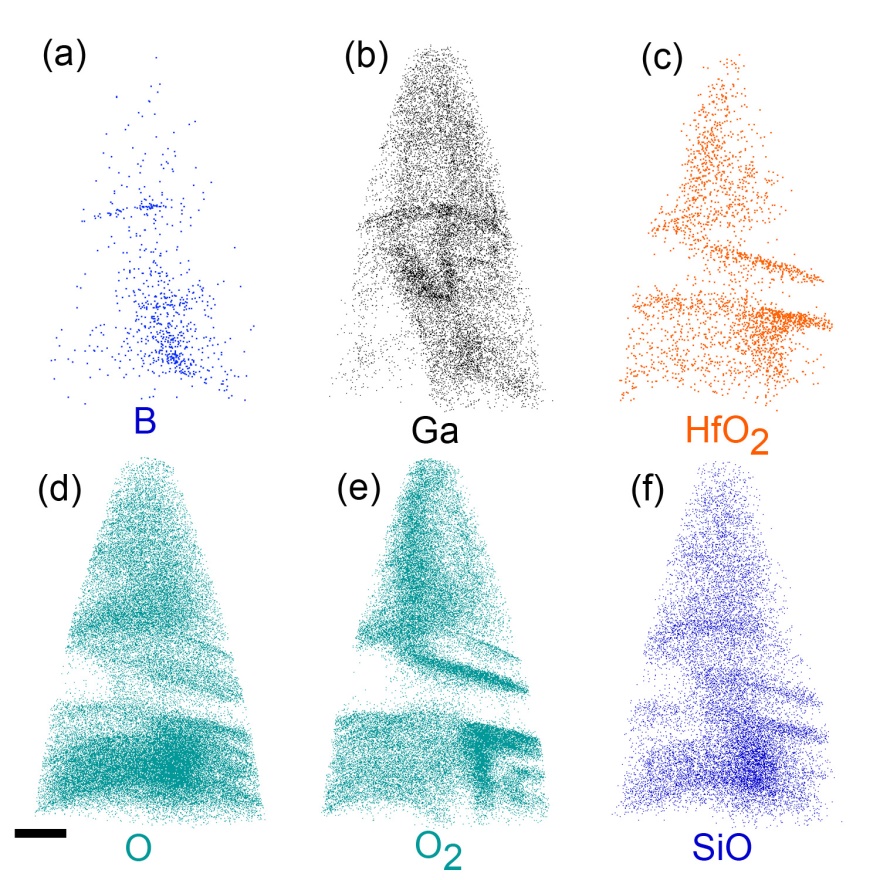


Figure S2: APT maps of B, Ga, HfO2, SiO, O and O2 for a PMOS fin.(a)The B shows a concentration close to the bottom of the map around the same region where the SiO and O signals are present. Boron is present closer to the source/drain contacts indicating the region near the contacts that has been captured in APT. (b) The Ga is from contamination during the ion milling process in the FIB (focused ion beam). (c) The HfO2 maps are shown here. They mimic the HfO signals (Figure 4(a) main text) both indicating the presence of a HfO2 dielectric layer. (d, e) The O and O2 maps are also shown. The O maps show a higher concentration at the bottom of the map between the two HfO walls, which along with the SiO maps (f) indicates the buried oxide layer between fins (Figure 1(a) main text. Scale bar is 30 nm.

**S3. Mass spectrum analysis for APT**

The mass spectrum for the PMOS and the NMOS maps obtained from APT is shown here. The labels are shown for the most intense peaks. Peaks that could not be identified are also shown with an asterisk. Maps not shown in Figure 3 and 4 of the main text and in Figure S1 and Figure S2 have a very low intensity and do not provide any new insights from what can be seen in other maps.

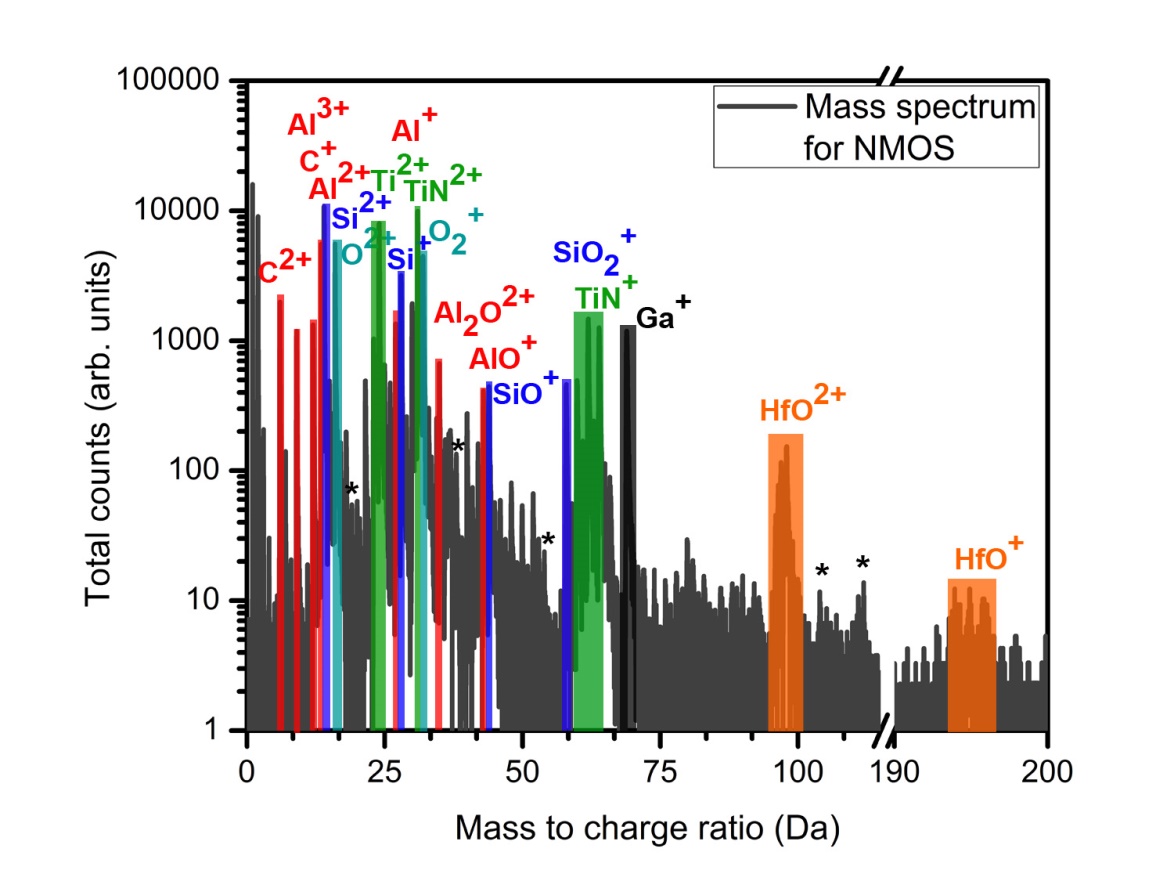


Figure S3: Major peaks analyzed in the mass spectrum of the NMOS device shown in Figure 3 of the main text. Chemical signatures of Si and all the dielectric layers are present in the mass spectrum.

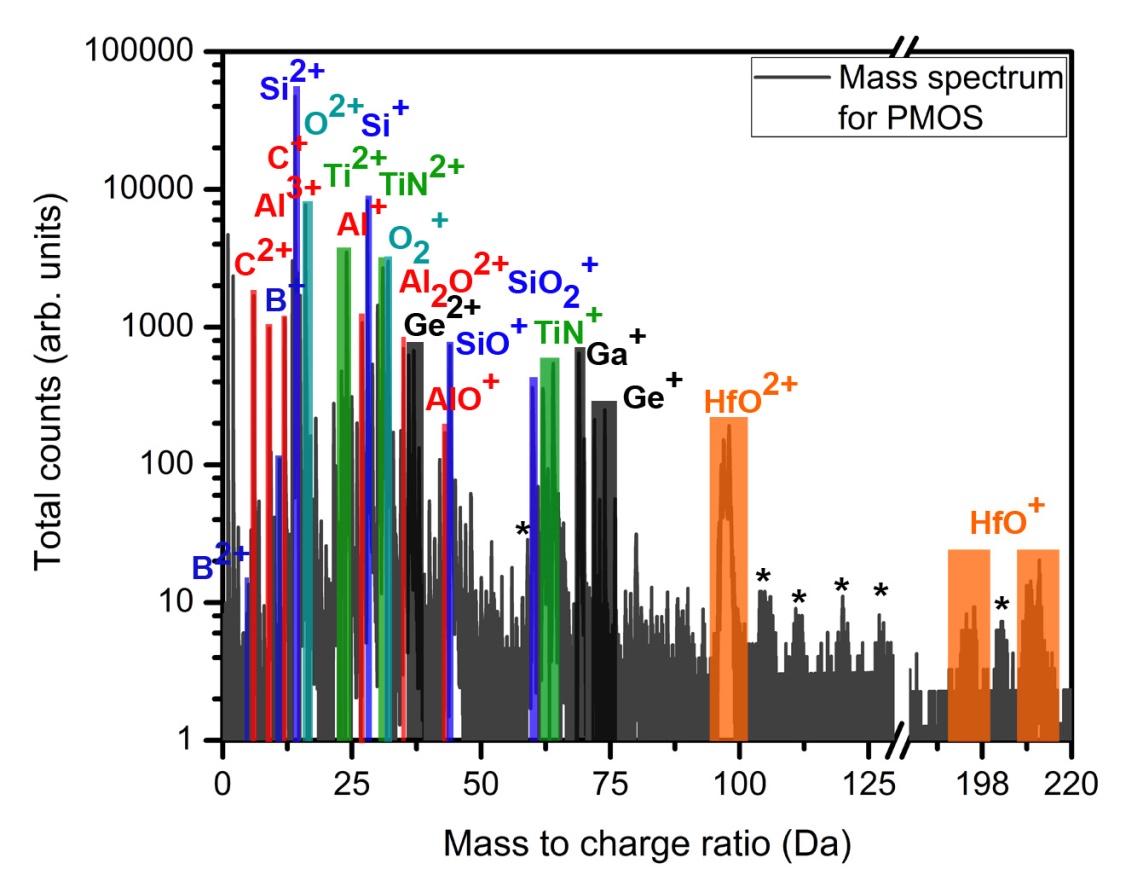
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Figure S4: Major peaks analyzed in the mass spectrum of the PMOS device shown in Figure 4 of the main text. Chemical signatures of Si, Ge and all the dielectric layers are present in the mass spectrum.

**S4. Sample preparation for APT**

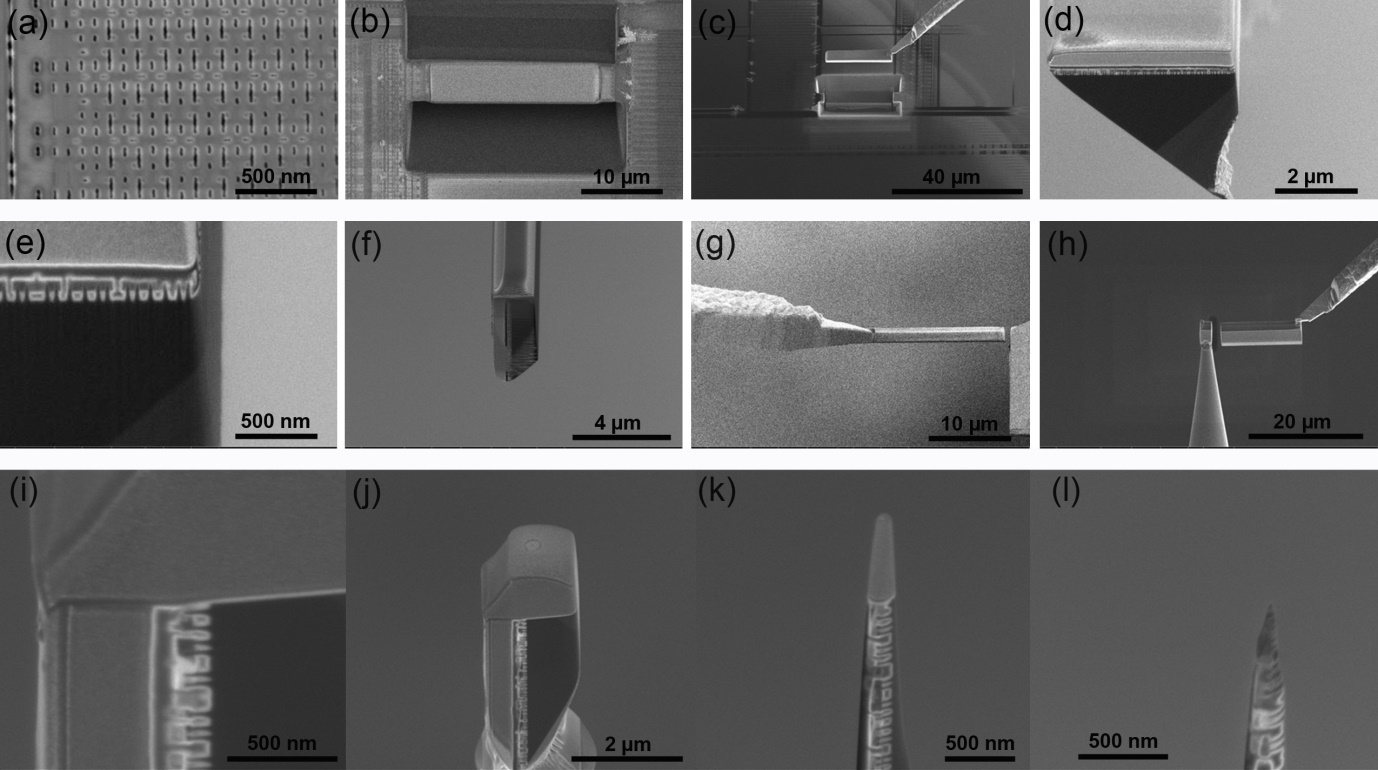


Figure S5: Cross-section sample preparation process for APT. The region of interest is identified from the SEM images (Figure 1 (b) main text) as seen in (a). A protection coating is deposited and milling trenches are made at an angle of 22° (b). The sample wedge is then picked up using a micromanipulator in situ (c); and the wedge is attached onto the ARM® module. As seen in (e), the right side wall is milled to ensure the transistor of interest is at this wall. The sample is now physically rotated 90° so that the fin of interest faces upwards and another wedge is made such that the fin aligns with the bottom end of the wedge section (f). This section is now picked up using a micromanipulator (g); and smaller sections of it are attached onto a Si microtip array (h). (i) Shows a magnified image of the fin at the apex of the smaller section with protective coatings on two sides and (j) shows one of the smaller sections attached to a microtip array. Annular milling is now carried out to reduce the end radius to less than 200 nm (k); and a final low current, low voltage milling step ensures a conical tip (l).

**S5. Sample preparation for TEM**

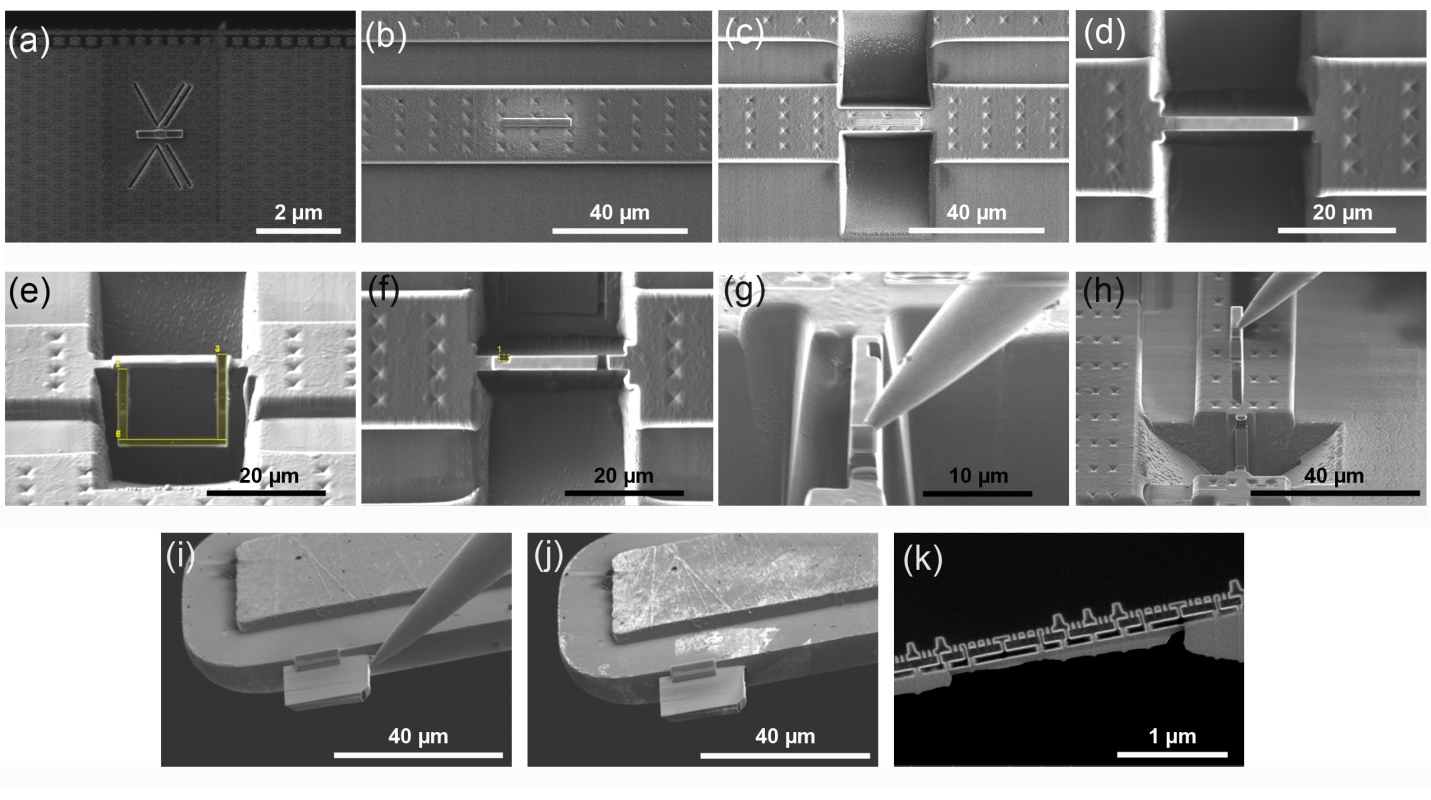


Figure S6: Sample preparation process for an inverted S/TEM cross-sectional lamella. The region of interest is protected by an e-beam induced deposition, which in addition to lines milled with the FIB column, serve as a fiducial as well, as seen in (a). A larger ion beam induced deposition is placed over the ROI (b). Bulk trenches are milled with the FIB on each side of the lamella as seen in (c). Using a lower ion beam current, the trenches are milled closer to the ROI (d). A “J” shaped pattern is milled with the FIB at 0° stage tilt to nearly free the lamella from the substrate (e). As seen in (f), a small box pattern is milled with the FIB to aid sample release in a subsequent step. The stage is now tilted to 0° and rotated 90° and a micromanipulator is brought in close proximity with the lamella and subsequently welded (g). The sample is then milled completely free from the substrate and the micromanipulator is used to transport the lamella (h). The micromanipulator is rotated 180° (not shown), and the lamella is welded to a TEM grid loaded in a specialized holder (i). The micromanipulator is milled free from the lamella (j) and the holder is manipulated (not shown) so the grid is oriented vertically. Finally, the lamella is thinned using successively lower ion beam accelerating voltages until a damage free lamella of the desired thickness is produced (k).

**S6. STEM-EDS additional maps**

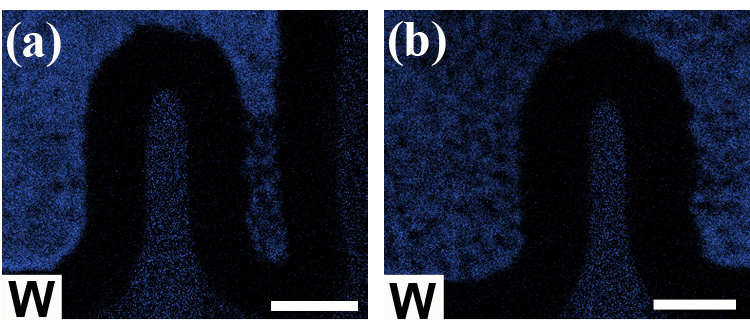
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Figure S6: EDS map of W for (a) NMOS and (b) PMOS fin respectively. Scale bar is 20 nm each.